IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. ..... Filed Concurrently Herewith
Filing Date ..... Filed Concurrently Herewith
Inventor ..... Keiji Jono et al.
Assignee ..... Micron Technology, Inc. and KMT Semiconductor, LTD
Group Art Unit ..... Unknown
Examiner ..... Unknown
Attorney's Docket No. KM1-001
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS

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Hollman

INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

The citations listed, copies attached, may be material to the examination of the subject application and are therefore submitted in compliance with the duty of disclosure defined in 37 CFR §1.56. The Examiner is requested to make these citations of official record in this application. No admission is made regarding whether all the submitted references are prior art.

The listed references are discussed in the specification under the heading "Background of the Invention".

The materials cited are presented to assist in and expedite examination of this application. The present invention is considered to be patentable over the cited materials. Expeditious examination and allowance of this application as a patent are therefore urged in order that the public may benefit from the disclosure and commercialization of the invention.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: Aug 31, 2000

Attorney: _____

Frederick M. Fliegel, Ph.D.
Reg. No.: 36,138

Form PTO-1449 | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		*Shallow Trench Isolation Characteristics with High-Density-Plasma Chemical Vapor Deposition Gap-Fill Oxide for Deep-Submicron CMOS*
			Technologies, Seung-Ho Lee et al., Jpn. J. Appl. Phys. Vol. 37 (1998), pp. 1222-1227.
	AS		*Impact of Shallow Trench Isolation on Reliability of Buried- and Surface-Chanel sub-μm PFET*, William Tonti et al., 1995 IEEE. pp. 24-29.
	AT		*Subbreakdown Drain Leakage Current in MOSFET*, J. Chen et al., 1987 IEEE, pp.515-517.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	AN							
	AO							
	AP							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		*Shallow Trench Isolation for advanced ULSI CMOS Technologies*, M. Nandakumar et al, Silicon Technology Development,
			Kilby Center, Texas Instruments, Undated, 4 pages.
	AS		
	AT		

EXAMINER	DATE CONSIDERED

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